

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

WHAT IS CLAIMED IS:

*Sub
a*

1. A shift clock signal generating apparatus for generating a shift clock signal having a prescribed phase difference from a reference clock signal, comprising:

5 a delay line receiving the reference clock signal and including a plurality of unit delay elements connected in cascade, wherein each of the unit delay elements provides a prescribed signal delay time, and the reference clock signal propagates in the delay line

10 while being successively delayed by the unit delay elements;

a shift clock signal output path;

a group of switches having first ends connected with output terminals of the unit delay elements respectively, and second ends connected with the shift clock signal output path, wherein when

15 specified one among the switches is in its on position, a delayed clock signal which results from delaying the reference clock signal by a prescribed time interval is transmitted via the specified switch to the shift clock signal output path as the shift clock signal; and

switch controlling means for determining the specified one

20 among the switches on the basis of data representing a phase difference of the shift clock signal from the reference clock signal, and for setting the specified switch in its on position.

2. A shift clock signal generating apparatus as recited in claim 1,

25 comprising a plurality of delay lines each being equal in structure to the previously-mentioned delay line, a plurality of groups of switches

each being equal in structure to the previously-mentioned group of switches, a plurality of shift clock signal output paths each being equal in structure to the previously-mentioned shift clock signal output path, and a plurality of switch controlling means each being equal in structure to the previously-mentioned switch controlling means to generate shift clock signals having prescribed phase differences from the reference clock signal, the prescribed phase differences being different from each other, wherein a number of the delay lines, a number of the groups of switches, a number of the shift clock signal output paths, and a number of the switch controlling means correspond to a number of the shift clock signals.

3. A shift clock signal generating apparatus as recited in claim 1, comprising a plurality of groups of switches each being equal in structure to the previously-mentioned group of switches, a plurality of shift clock signal output paths each being equal in structure to the previously-mentioned shift clock signal output path, and a plurality of switch controlling means each being equal in structure to the previously-mentioned switch controlling means to generate shift clock signals having prescribed phase differences from the reference clock signal, the prescribed phase differences being different from each other, wherein first ends of the switches in each of the groups are connected with the output terminals of the unit delay elements respectively, and wherein a number of the groups of switches, a number of the shift clock signal output paths, and a number of the switch controlling means correspond to a

number of the shift clock signals.

4. A shift clock signal generating apparatus as recited in claim 3, wherein the switch groups are connected with the output terminals of ones among the unit delay elements in correspondence with the prescribed phase differences of the related shift clock signals from the reference clock signal.
5. A shift clock signal generating apparatus as recited in claim 4, wherein the unit delay elements are separated into groups having a number equal to a number of the shift clock signals, and the switch groups are connected with unit delay elements in the corresponding unit-delay-element groups respectively.
- 10
- 15 6. A shift clock signal generating apparatus as recited in claim 1, further comprising a reference clock signal output path for outputting the reference clock signal to an external as it is.
- 20 7. A shift clock signal generating apparatus as recited in claim 1, wherein each of the unit delay elements includes a gate circuit for providing the prescribed signal delay time.
- 25 8. A shift clock signal generating apparatus as recited in claim 1, wherein the switch controlling means operates for determining the specified one among the switches on the basis of period data and ratio data, the period data representing a numeric value of a period

of the reference clock signal while a time resolution is given by the prescribed signal delay time provided by each of the unit delay elements, the ratio data representing a ratio between a delay time of the shift clock signal relative to the reference clock signal and the 5 period of the reference clock signal.

9. A shift clock signal generating apparatus as recited in claim 8, wherein the ratio represented by the ratio data is equal to $y/(x+1)$, and "x" denotes a predetermined natural number and "y" denotes a 10 natural number in a range of "1" to "x".

10. A shift clock signal generating apparatus as recited in claim 9, further comprising:

a ring delay line including a plurality of unit delay elements 15 connected in a closed loop and being equal in characteristics to the unit delay elements in the previously-mentioned delay line, wherein a pulse signal circulates through the ring delay line while being delayed by the unit delay elements; and

time A/D converting means for counting a number of times 20 the pulse signal goes round the ring delay line, for generating the period data in response to the counted number of times, and for feeding the period data to the switch controlling means.

11. A shift clock signal generating apparatus as recited in claim 8, 25 further comprising a digitally controlled oscillation circuit for outputting a signal having a period controllable while a time

resolution is given by the prescribed signal delay time provided by each of the unit delay elements, the digitally controlled oscillation circuit using control data in controlling the period of the signal outputted therefrom, the delay line receiving the signal outputted from the digitally controlled oscillation circuit as the reference clock signal, the switch controlling means operating for using the control data as the period data.

12. A shift clock signal generating apparatus as recited in claim 8, further comprising a digitally controlled oscillation circuit for outputting a signal having a period controllable while a time resolution is given by the prescribed signal delay time provided by each of the unit delay elements, the digitally controlled oscillation circuit using control data in controlling the period of the signal outputted therefrom, and a frequency divider circuit for dividing a frequency of the signal outputted from the digitally controlled oscillation circuit to generate the reference clock signal having a duty cycle of 50%, the delay line receiving the reference clock signal generated by the frequency divider circuit, the switch controlling means operating for doubling a period represented by the control data to calculate the period of the reference clock signal and for generating the period data in accordance with the calculated period.

13. A shift clock signal generating apparatus as recited in claim 11, wherein the digitally controlled oscillation circuit includes:

100-000-0000-0000

J.Y

a ring delay line including a plurality of unit delay elements connected in a closed loop and being equal in characteristics to the unit delay elements in the previously-mentioned delay line, wherein a pulse signal circulates through the ring delay line while being delayed by the unit delay elements;

5 delayed by the unit delay elements;

time A/D converting means for counting a number of times the pulse signal goes round the ring delay line, for generating the period data in response to the counted number of times, and for outputting the period data;

10 dividing means for dividing a value of the period data outputted from the time A/D converting means by a preset number to generate the control data; and

15 signal outputting means for comparing a value of the control data and a number of times the pulse signal passes through a unit delay element in the ring delay line, and for outputting a prescribed-pulsewidth signal each time the value of the control data and the number of times become equal to each other.

14. A time measurement apparatus comprising:

20 a shift clock signal generating means for generating a plurality of shift clock signals in response to a reference clock signal, the shift clock signals having a period equal to a period of the reference clock signal, the shift clock signals having phases different from each other;

25 signal inputting means for converting an input signal into binary signals in response to the shift clock signals generated by the

ପାତା ୧୦୫

shift clock signal generating means respectively, the input signal containing a pulse train of a pseudo random noise code;

correlation calculating means for calculating correlations between the pseudo random noise code and the binary signals
5 generated by the signal inputting means;

detecting means for detecting a moment at which a peak of the correlations calculated by the correlation calculating means occurs; and

10 measuring a time interval from a prescribed moment to a moment of occurrence of the pulse train in the input signal on the basis of the moment detected by the detecting means.

15. A time measurement apparatus as recited in claim 14, wherein a number of the shift clock signals is equal to a
15 predetermined integer "n", and differences between the phases of the shift clock signals are equal to the reference-clock-signal period divided by the predetermined integer "n".

16. A time measurement apparatus as recited in claim 14,
20 wherein the correlations calculated by the correlation calculating means are in pairs each having correlations related to two among the shift clock signals which have phases most different from each other, and further comprising averaging means for averaging correlations in each of the pairs into a mean correlation, the
25 detecting means operating for detecting a moment at which a peak of the mean correlations generated by the averaging means occurs

as an indication of the moment of occurrence of the pulse train in the input signal.

5 17. A time measurement apparatus as recited in claim 14,
wherein the correlation calculating means includes synchronizing
means for sampling the binary signals generated by the signal
inputting means into second binary signals in response to the
reference clock signal, and means for calculating correlations
between the pseudo random noise code and the second binary
signals, the correlation calculating means and the detecting means
10 operating in response to the reference clock signal.

15 18. A time measurement apparatus as recited in claim 17,
wherein the detecting means operates for detecting a moment at
which a peak of the correlations calculated by the correlation
calculating means occurs on the basis of one of (1) a moment at
which one of the correlations exceeds a preset threshold value and
20 (2) a phase difference between the reference clock signal and one
among the shift clock signals which corresponds to the correlation
exceeding the preset threshold value.

25 19. A time measurement apparatus as recited in claim 18,
wherein the detecting means operates for detecting a moment at
which a peak of the correlations calculated by the correlation
calculating means occurs on the basis of a moment at which one of
the correlations first exceeds a preset threshold value.

20. A spread-spectrum distance measurement apparatus comprising:

5 pulse train generating means for generating a pulse train of a pseudo random noise code in synchronism with a reference clock signal, the pseudo random noise code having a prescribed bit length;

10 transmitting means for transmitting an electromagnetic wave modulated in accordance with the pulse train generated by the pulse train generating means;

15 receiving means for receiving an echo wave caused by reflection of the electromagnetic wave transmitted by the transmitting means at an object to be measured, and for converting the received echo wave into a received pulse train signal;

20 time measuring means for measuring a time interval from a moment of transmission of the electromagnetic wave from the transmitting means to a moment of reception of the echo wave by the receiving means on the basis of the pseudo random noise code and the received pulse train signal; and

25 distance calculating means for calculating a distance to the object on the basis of the time interval measured by the time measuring means;

 wherein the time measuring means comprises the time measurement apparatus of claim 14.

25

21. A spread-spectrum distance measurement apparatus as

recited in claim 20, wherein the pulse train generating means operates for generating the pulse train of the pseudo random noise code a plurality of times, and the time measuring means operates for measuring the time interval a plurality of times, and the distance calculating means operates for averaging the time intervals measured by the time measuring means into a mean time interval, and for calculating the distance to the object on the basis of the mean time interval.

10 22. A spread-spectrum distance measurement apparatus as recited in claim 21, wherein the time measuring means operates for determining a center among the time intervals measured by the time measuring means, for excluding one or more among the time intervals which deviate from the center by greater than a prescribed 15 value to get remaining time intervals, and for averaging the remaining time intervals into the mean time interval.

4321247-2